WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first chip having an electrically rewritable nonvolatile memory,

a second chip including a memory having therein a redundant circuit, and

a substrate on which said first chip and second chip are mounted,

wherein information required for utilizing said redundant circuit in place of a faulty portion in said memory on said second chip is stored in said nonvolatile memory on said first chip, and said redundant circuit is utilized in place of the faulty portion in said memory on said second chip based on the information stored in said nonvolatile memory.

2. The semiconductor device according to claim 1, wherein said second chip further comprises a circuit for memory test having a nonvolatile memory, wherein said nonvolatile memory of said second chip stores,

a test program for detecting whether or not there is a faulty portion in said memory on said second chip;

a repair analysis program for identifying the faulty portion when the test program detects that there is a faulty portion in said memory on said second chip, and determining

a portion in said redundant circuit that is to be utilized in place of the faulty portion; and

a software repair program for writing information required for utilizing the determined portion in said redundant circuit in place of the faulty portion identified by the repair analysis program in said nonvolatile memory on said first chip.

3. The semiconductor device according to claim 2, wherein said nonvolatile memory in said circuit for memory test is rewritable.

4. The semiconductor device according to claim 1, further comprising a third chip, said third chip being mounted on said substrate, said third chip including a circuit for memory test having a nonvolatile memory, wherein said nonvolatile memory on said third chip stores,

a test program for detecting whether or not there is a faulty portion in said memory on said second chip;

a repair analysis program for identifying the faulty portion when the test program detects that there is a faulty portion in said memory on said second chip, and determining a portion in said redundant circuit that is to be utilized in place of the faulty portion; and

a software repair program for writing information

required for utilizing the determined portion in said redundant circuit in place of the faulty portion identified by the repair analysis program in said nonvolatile memory on said first chip.

5. The semiconductor device according to claim 4, wherein said nonvolatile memory in said circuit for memory test is rewritable.

6. The semiconductor device according to claim 1, wherein said first chip and second chip are stacked on said substrate.

7. The semiconductor device according to claim 4, wherein said first chip, said second chip, and third chip are stacked on said substrate.

8. A semiconductor device comprising:

a first chip having an electrically rewritable nonvolatile memory,

a second chip including a memory,

a third chip having a redundant circuit, and

a substrate on which said first chip, said second chip, and said third chip are mounted,

wherein information required for utilizing said redundant circuit on said third chip in place of a faulty

portion in said memory on said second chip is stored in said nonvolatile memory on said first chip, and said redundant circuit on said third chip is utilized in place of the faulty portion in said memory on said second chip based on the information stored in said nonvolatile memory on said first chip.

9. The semiconductor device according to claim 5, wherein said second chip further comprises a circuit for memory test having a nonvolatile memory, wherein said nonvolatile memory of said second chip stores,

a test program for detecting whether or not there is a faulty portion in said memory on said second chip;

a repair analysis program for identifying the faulty portion when the test program detects that there is a faulty portion in said memory on said second chip, and determining a position of a portion in said redundant circuit that is to be utilized in place of the faulty portion; and

a software repair program for writing information required for utilizing the determined portion in said redundant circuit in place of the faulty portion identified by the repair analysis program in said nonvolatile memory on said first chip.

10. The semiconductor device according to claim 9, wherein said nonvolatile memory in said circuit for memory test is rewritable.

11. The semiconductor device according to claim 8, further comprising a fourth chip, said fourth chip being mounted on said substrate, said fourth chip including a circuit for memory test having a nonvolatile memory, wherein said nonvolatile memory on said fourth chip stores,

a test program for detecting whether or not there is a faulty portion in said memory on said second chip;

a repair analysis program for identifying the faulty portion when the test program detects that there is a faulty portion in said memory on said second chip, and determining a position of a portion in said redundant circuit that is to be utilized in place of the faulty portion; and

a software repair program for writing information required for utilizing the determined portion in said redundant circuit in place of the faulty portion identified by the repair analysis program in said nonvolatile memory on said first chip.

12. The semiconductor device according to claim 11, wherein said nonvolatile memory in said circuit for memory test is rewritable.

13. The semiconductor device according to claim 8, wherein said first chip, said second chip, and third chip are stacked on said substrate.